EXHIBIT D

Synopsys Draft Patent Application[1]	Specification Of '446 Patent (Also Contained in '438 Patent)
SYNOPSYS DRAFT PAT. APP. AT 2 The major problem with the ***conventional approach*** is that the net length and hence the cell delay is not known ***until after placement***.	**'446 PATENT AT 1:46-47** Thus, under the ***conventional*** design ***approach***, timing closure is not certain ***until after placement***.
SYNOPSYS DRAFT PAT. APP. AT 2-3 Before placement, ***net length*** must be ***estimated***. This is usually done with ***an estimation function or table which gives the load of a net based on*** its ***fanout***. Experience has shown that it is very difficult to ***estimate*** the length of the nets ***accurately***.	**'446 PATENT AT 1:37-40** While ***net lengths*** have been ***estimated*** prior to placement by use of ***an estimation function or table which gives the load value of a net based on*** the number of ***fanout*** gates, this ***estimation*** function is usually ***inaccurate***.
SYNOPSYS DRAFT PAT. APP. AT 3 The result is unpleasant surprises ***after placement*** step 105. ***Some nets turn out to be longer than expected***, and because of the ***longer delays***, the ***timing constraints*** are not met. ***Timing closure is not certain until after*** step 105.	**'446 PATENT AT 1:41:46** This difficulty in accurately predicting net lengths leads to unpredictable delay effects ***after*** cell ***placement*** occurs. For example, ***some nets turn out to be longer in length than expected***. These longer nets cause ***longer delays*** which prevent satisfaction of ***timing constraints*** in the digital circuit. Thus, under the conventional design approach, ***timing closure is not certain until after*** placement.

[1] Note that page numbers do not appear on the Draft Patent Application.

Synopsys Draft Patent Application[1]	Specification Of `446 Patent (Also Contained in '438 Patent)
SYNOPSYS DRAFT PAT. APP. AT 3 If ***timing closure*** is not ***achieved*** the options the ***designer*** has are ***expens***ive and unreliable. He may choose to ***fix*** the ***design manually, which is difficult and time consuming, because the automatically optimized network*** is hard to ***understand***. He may choose to ***change*** his ***HDL specification and repeat the*** synthesis ***process***. Again ***timing closure will not be certain until after placement***, which means that the entire ***process*** needs to be traversed ***before the designer*** knows ***if*** his ***HDL changes were successful***.	**`446 PATENT AT 1:48-60** Failure to ***achieve timing closure*** after placement leads to additional ***expens***es and other problems for the ***designer***. To correct for failure to achieve timing closure, the ***designer*** has the option of ***fix***ing ***the design manually, which is difficult and time consuming because the automatically optimized*** digital ***network*** is not easy ***to understand***. As a second option, the designer may ***change*** the Hardware Description Language ***(HDL) specification and repeat the*** design ***process***. However, ***timing closure will*** again ***not be certain until after placement***. Thus, the design ***process*** must again be repeated ***before the designer*** can determine ***if*** the ***HDL*** specification ***changes were successful*** in enabling timing closure.
SYNOPSYS DRAFT PAT. APP. AT 3 ***A common method*** of ***dealing with inaccurate net load estimates is*** to use ***net load estimates*** which are ***considerably larger than*** accurate ***estimate***s. This ***causes the sizes of the cells to be considerably larger then necessary*** but reduces the ***probability of*** not ***meeting*** the ***timing constraints after placement***. Clearly using cells with ***sizes which are larger then necessary*** is ***wasteful in both silicon area and power consumption***. The ***chips*** thus synthesized will be ***larger***, cost ***more to produce and use more electrical power then necessary***.	**`446 PATENT AT 1:61-2:3** ***A common method*** for ***dealing with inaccurate net load estimates is*** by ***estimat***ing the ***net load*** at a ***considerably larger*** value ***than*** typically ***estimate***d. Although this method increases the ***probability of meeting timing constraints after placement***, it ***causes the sizes of the gates to be considerably larger than necessary***. Gates ***which are larger than*** the ***necessary size*** are ***wasteful in both silicon area and power consumption***. This leads to ***chips*** which are ***larger, more*** expensive ***to produce, and use more electrical power than necessary***.
SYNOPSYS DRAFT PAT. APP. AT 3 A second ***problem with the conventional approach*** is that the effect of synthesis decisions is hard to calculate. ***Perform***ing ***timing analysis during optimization is very time consuming, and accounts for most of the run time of conventional synthesis systems***.	**`446 PATENT AT 2:4-9** Another ***problem with the conventional*** circuit design ***approach*** concerns the timing analysis required ***during optimization*** and during placement. The ***timing analysis perform***ed throughout the conventional circuit design process ***is very time consuming, and accounts for most of the run time of*** a ***conventional*** circuit design ***system***.

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SYNOPSYS DRAFT PAT. APP. AT 4 In step 105 the placement program will ***modify*** the ***net lengths***. ***Depending on*** which ***location*** was ***chosen for each*** cell, the ***length*** of ***each net*** can be different. ***As*** the ***length*** differs, ***the capacitive load of the net changes***, and as a result, the delay of the cell driving the net changes. ***Therefore the delays which were carefully optimized during the logic*** synthesis, ***are very different after placement***, and the ***optimization*** of the ***network*** is not very good.	'446 PATENT AT 2:12-19 ***Depending on*** the ***location chosen for each*** gate, each net ***length*** may be ***modified***. ***As each net length*** is modified, ***the capacitive load of the net*** will ***change***. ***Therefore, the delays, which were carefully optimized during the logic*** design, ***are very different*** in value ***after*** cell ***placement***, thereby contributing to poor ***network optimization***.
SYNOPSYS DRAFT PAT. APP. AT 4 ***Much of the progress in the state of the art can be characterized as increased integration***. This is represented in figure 1 as various feedback paths, which repeat and alternate steps. The general direction has been towards programs which do structuring, mapping, sizing and placement simultaneously. It ***has led to increasingly complex software systems which are slow and difficult to design and maintain.***	'446 PATENT AT 2:20-23 Additionally, ***much of the progress in the state of the art for digital circuit design can be characterized as increased integration*** which ***has led to increasingly complex software systems which are slow, and difficult to design and maintain.***
SYNOPSYS DRAFT PAT. APP. AT 4 ***Iterating between placement and sizing*** has been especially hard to execute because placement programs are not sold by the same design automation software vendors as ***logic synthesis programs***. Also they are not run by the same users: the logic synthesis program is often run by the ***designer, who also wrote the HDL specification***. The ***placement program is often*** run ***by the silicon chip manufacturer, after the design is*** considered ***complete***.	'446 PATENT AT 2:24-30 A further disadvantage with conventional design approaches is in the difficulty of ***iterating between placement and sizing***, since the ***logic synthesis program*** is often operated by the logic ***designer who also wrote the HDL specification***, but the ***placement program is often*** operated ***by the silicon chip manufacturer, after the design is complete***.

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SYNOPSYS DRAFT PAT. APP. AT 6 The ***present invention maintains timing closure*** after it has been achieved by ***adjust***ing the ***size*** of the cell ***during or after placement***. The ***adjustment***s ***compensate for the fact that the placement algorithm*** can ***assign different net lengths to different nets and that these lengths are difficult to predict*** before ***placement***.	**'446 PATENT AT 16:23-29** According to the ***present invention***, ***timing closure*** is ***maintain***ed after placement occurs of cells 836. To ***maintain timing closure***, the ***size*** of a particular gate may be ***adjust***ed ***during or after placement***. This ***adjustment compensates for the fact that placement algorithm*** may ***assign different net lengths to different nets, and that these*** different net ***lengths are difficult to predict*** prior to the ***placement*** step.
SYNOPSYS DRAFT PAT. APP. AT 8 Wherever possible, the same ***reference numbers*** will be used throughout the ***drawings*** to ***refer*** to the same or like ***parts***.	**'446 PATENT AT 4:59-63** ***Refer***ring in detail now to the ***drawings*** wherein similar ***parts*** or steps of the present invention are identified by like ***reference numerals***, there is seen in FIG. 1 a schematic diagram of a host computer system 100 which is capable of implementing the present invention.
SYNOPSYS DRAFT PAT. APP. AT 9 The cells ***can be combinational*** "***gates***" 207, 208, 209, ***whose function is represented as*** an ***expression*** in the ***Boolean*** algebra, using ***AND, OR and NOT operators***, or the cells ***can be registers*** 205, 206.	**'446 PATENT AT 5:13-17** The gates ***can be combinational gates whose function is represented as Boolean expression*** based on, for example, the ***operators AND, OR and NOT***. The gates ***can*** also ***be registers***.
SYNOPSYS DRAFT PAT. APP. AT 9 ***Each*** cell (***e.g.***, 208) ***has one or more inputs*** 212, 213, ***and a single output*** 214.	**'446 PATENT AT 5:18-19** ***Each*** gate (***e.g.***, gate j) ***has one or more input*** 155 ***and a single output*** 160.

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SYNOPSYS DRAFT PAT. APP. AT 9 Cells ***whose inputs are connected to the output of a*** cell ***are called the fanin of the latter*** cell. Cells ***whose inputs are connected to the output of a*** cell ***are called the fanout of the latter*** cell.	**`446 PATENT AT 5:26-32** Gates ***whose outputs are connected to the inputs of a*** gate ***are*** collectively ***called the "fanin" of the latter*** gate. Thus, the gate k is in the fanin of the gate i. Gates ***whose inputs are connected to the output of a*** gate ***are*** collectively ***called the "fanout" of the latter*** gate. Thus, the gate j is in the fanout of the gate i.
SYNOPSYS DRAFT PAT. APP. AT 9 ***The digital*** network ***performs a logic "function" by processing digital binary input data in a number of cycles. The input data is presented to the*** network on its ****primary inputs**** 201, 202, ***and the result of the computation of the*** network ***function is presented at the ****primary outputs**** 203, 204, of the network. ***The computation of the function*** takes ***one or more cycles. During each cycle the gate functions are calculated. The results are stored in*** the ***registers for use in the next cycle.***	**`446 PATENT AT 5:33-41** ***The digital*** circuit 150 ***performs a logic function by processing digital binary input data in a number of cycles. The input data is presented to the*** digital circuit 150 at the ***primary inputs*** 170, ***and the result of the computation of the*** digital circuit ***function is presented at the primary outputs*** 175. Typically, ***the computation of the*** digital circuit ***function*** requires ***one or more cycles. During each cycle, the gate functions are calculated,*** and ***the*** calculation ***results are stored in registers for use in the next cycle.***
SYNOPSYS DRAFT PAT. APP. AT 10 The "***arrival time" of the data at a gate is computed by taking the maximum arrival time of*** its ***fanin*** cells each increased by ***the delay from the input pin to the output pin.***	**`446 PATENT AT 9:55-58** (An ***arrival time of the data at a gate is computed by taking the maximum arrival time of*** the ***fanin*** gates plus ***the delay*** measured ***from the input pin to the output pin*** of the gate).

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SYNOPSYS DRAFT PAT. APP. AT 11 The difference between the required time and the arrival time is the ***slack***. If the arrival time is smaller than the required time, ***the timing constraints are met***, and the ***slack is positive***. If the arrival time is larger than the required time, the timing constraints are not met, and the slack is negative. The arrival time and required time may be different depending on whether the data is zero (0) or one (1). There also may be multiple arrival times and multiple required times to model a variety of timing constraints. ***All slacks can be summarized*** as a ***single worst slack number***, called ***the *network slack****. ***Timing closure is achieved if the network slack is non-negative.***	**`446 PATENT AT 13:27-34** This determination is made by subtracting the delay of the buffer from the "local ***slack***", to give the value of the predicted slack after buffer insertion. ***Slack is*** zero or ***positive*** if ***the timing constraints are met***. In addition, ***all slacks*** in the circuit ***can be summarized by the "network slack"*** which is the ***single "worst" slack number***. ***If the network slack is non-negative***, then the ***timing closure is achieved***.
SYNOPSYS DRAFT PAT. APP. AT 11 It is important to note that the dependency on size and load can be captured as the dependency on a single parameter C/S, and ***the delay D is non-negative and*** monotonically ***increas***ing with ***C/S***.	**`446 PATENT AT 6:38-43** The delay D of a gate can be approximated by equation (1): D=f(C/S) (1) ***The delay D is non-negative and increas***es as the ***C/S*** value increases.
SYNOPSYS DRAFT PAT. APP. AT 11 ***The delay may be different for different inputs of the gate and it may be different for the falling and the rising transition.***	**`446 PATENT AT 6:58-61** ***The delay*** D value ***may*** also ***be different for different inputs of the gate and it may*** also ***be different for the falling transition and rising transition*** of a signal propagating through the gate.
SYNOPSYS DRAFT PAT. APP. AT 12 ***The library analysis will determine a good value for C/S for each*** cell ***in the library***.	**`446 PATENT AT 6:63-65** ***The library analysis will determine a "good" value for C/S for each gate in the library*** based on gain considerations.

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SYNOPSYS DRAFT PAT. APP. AT 13 Mostly these optimizations ***change the structure of the*** network, ***and the Boolean functions of the*** cells, ***without changing the overall function of the*** network. The types of ***optimizations*** that should be performed are ***behavioral optimization such as resource sharing, sequential optimizations such as retiming, algebraic optimizations such as kernel extraction and Boolean optimizations such as redundancy removal***. These is a large amount of literature on how each of these ***classes of optimizations*** can be performed.	**'446 PATENT AT 9:13-22** During this step, ***the structure of the*** circuit ***and the Boolean functions of the*** gates are ***changed*** to reduce the total number of connections, ***without changing the overall function of the*** circuit. Structural ***optimizations*** can include ***behavioral optimizations (such as resource sharing), sequential optimizations (such as retiming), algebraic optimizations (such as kernel extraction), and Boolean optimizations (such as redundancy removal)***. The ***classes of optimizations*** above are well known to those skilled in the art.
SYNOPSYS DRAFT PAT. APP. AT 13 Following the library independent optimizations, the network ***is mapped to a library of cells***. This means that ***the logic functions of the*** cells ***are implemented with actual cells from the library.***	**'446 PATENT AT 9:25-27** In step 210 (FIG. 4), the circuit ***is mapped to a library*** 209 ***of cells***. Thus, ***the logic functions of the*** circuit gates ***are implemented with actual cells from the library*** 209.
SYNOPSYS DRAFT PAT. APP. AT 14 For example, we can ***use*** the "boundary move" ***transformation to reduce the number of levels in the logic in the*** mapped network. The boundary move ***transform***, illustrated in fig x, ***reduces the number of levels by bringing*** connection x ***forward***.	**'446 PATENT AT 10:45-49** A local ***transformation*** is then ***used to reduce the number of levels in the logic in the*** gate chain circuit 550. The result of the ***transformation*** is shown as gate chain circuit 550' in FIG. 7B. ***The number of levels*** in the logic is ***reduced by bringing*** the gate 555 ***forward***.
SYNOPSYS DRAFT PAT. APP. AT 14 To make the change legal ***it is necessary that gates*** x, y and z ***are fanout free. If not, they*** must be ***made fanout free*** by making a ***copy***.	**'446 PATENT AT 10:59-62** In order for the transformation shown in FIG. 7B to be valid, ***it is necessary that gates*** 555, 560, and 565 ***are fanout free. If*** the gates 555, 560, and 565 are ***not*** fanout free, then ***they*** are ***made fanout free*** through ***copy***ing logic.

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SYNOPSYS DRAFT PAT. APP. AT 14-15 In the ***conventional*** approach to ***logic*** synthesis, ***copying logic will increase the load on gates*** x, x, x and therefore increase the delay. ***To predict*** if ***the transformation*** will ***improve delay***, or hurt delay, ***it*** was ***necessary to run a complete static timing analysis with accurate delay models***. ***If the*** change ***actually*** worsened the ***delay***, ***then the*** change ***would be undone***.	**`446 PATENT AT 11:4-13** Under ***conventional logic*** design, ***copying logic will increase the load on*** the ***gates*** whose outputs are connected to lines 575, 580, 585, and 590. In the example of FIG. 7B, the copying logic 555' ***increases the load on the gates*** whose outputs are connected to lines 575 and 580. ***To predict*** whether or not ***the transformation improved delay***, ***it*** is ***necessary to run a complete static timing analysis with accurate delay models***. ***If the*** transformation (from circuit 550 to 550') were ***actually*** harmful to ***delay***, ***then the*** transformation ***would*** have to ***be undone***.
SYNOPSYS DRAFT PAT. APP. AT 15 ***In the constant delay model approach, the effect of this*** change ***can be easily predicted***. Note that ***changes in loads do not affect delay***. ***The only change*** that is ***affects delay, is the change of the fanin of gate*** xxx. ***The delay can*** easily ***be predicted by simple addition of gate delays.***	**`446 PATENT AT 10:49-58** ***In the constant delay model approach, the effect of this*** transformation ***can be easily predicted***. ***Changes in the gate loads do not affect delay,*** since delay is maintained as constant while gate size will be adjusted (during or after placement) to compensate for the load change. ***The only change*** which ***affects delay*** (of the gate chain circuit 550) ***is the change of the fanin of gate*** 555. ***This delay*** change ***can be predicted by simple addition of gate delays*** provided by the fanins connected at lines 590, 575, and 580 (see gate chain circuit 550' in FIG. 7B).
SYNOPSYS DRAFT PAT. APP. AT 15 The ***net load*** consists of the ***load*** of the ***net***, which ***can be estimated using a conventional net load model, plus any other fixed load, such as the load of*** a ***primary output***.	**`446 PATENT AT 11:26-30** The parameter w represents the ***net*** (wire) ***load*** for a given gate i (wherein the ***net load can be estimated using a conventional net load model*** such as the above-mentioned fanout-based model) ***plus any other fixed load such as the load of*** the ***primary output*** of the circuit implementation.

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SYNOPSYS DRAFT PAT. APP. AT 15 In ***a combinational network*** this can be achieved by starting ***at the primary outputs and traversing the*** network ***in a levelized order towards the primary inputs.***	**`446 PATENT AT 11:48-52** If the digital circuit is ***a combinational network*** (see, e.g. circuit 150 in FIG. 2), then gate load calculation initiates ***at the primary outputs*** 175 ***and traverses the*** circuit ***in a leveled order toward the primary inputs*** 170.
SYNOPSYS DRAFT PAT. APP. AT 15-16 In ***a sequential network there may be one or more loops, resulting a cyclic dependency***: ***there is no rightmost*** cell. In this case the computation ***can start anywhere in the cycle, and*** repeats ***the cycle several times, until the capacitances converge*** and the error is ***sufficiently small.*** It is possible that this iteration will ***not converge and*** that the ***capacitance*** will ***increase*** in every iteration, ***by progressively larger amounts***. This situation is ***detected*** by requiring the increment to be smaller then ***a preset maximum after a fixed number of*** iterations. The iteration does ***not converge*** if the network is ***an infeasible solution***: The current network can***not*** be ***expected to work at*** this ***speed because*** its ***gain is too small. Changes*** need to be made to the network to ***increase the gain***, which ***will usually*** mean ***increasing*** the ***delay*** of the network as well.	**`446 PATENT AT 11:53-12:4** If the digital circuit is ***a sequential network*** (see, e.g., circuit 180 of FIG. 3), then ***there may be one or more loops*** (e.g., loop 182) which ***result*** in ***a cyclic dependency*** (i.e., ***there is no "rightmost"*** gate). Gate load calculation ***can start anywhere in the cycle, and*** calculation in ***the cycle*** is performed ***several times until the*** load ***capacitance*** values ***converge*** or have ***sufficiently small*** differences. However, a condition may exist when the load ***capacitance*** values do ***not converge and increase by progressively larger amounts*** every cycle calculation. This increase in load capacitance values can be ***detected*** if the calculated load values exceed ***a preset maximum*** value ***after a fixed number of*** cycle calculations. When the calculated load values do ***not converge***, then the particular circuit 180 has ***an infeasible solution***, which indicates that the digital circuit is ***not expected to work at*** the set ***speed because*** the circuit ***gain is too small. Changes*** are required to ***increase the*** circuit ***gain***, and these changes ***will usually*** lead to an increase in circuit ***delay***.

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SYNOPSYS DRAFT PAT. APP. AT 16 After the loads have been calculated the ***size*** can be calculated ***by dividing the actual load by the predetermined typical load***. The input capacitance can be calculated by multiplying the unit gate input capacitance by the size. The ratio of these numbers is the ***size*** of the ***gate***. ***The size is a scale factor, which*** can be applied to the area of ***the gate***, to give ***the area of the sized gate. The area of the*** network ***can be estimated*** as ***the sum total*** of the ***areas of the sized gates, plus the net area*** as ***estimated from the total length of all nets***.	**'446 PATENT AT 12:5-20** In the above example, the ***size*** S of a gate i is determined ***by dividing the actual load*** C_i ***by the predetermined typical load*** C/S of the gate i. The size S is a scale factor which is applied to all transistor channel widths of a gate in order to determine the area of the "***sized gate***". ***The size*** S ***is*** also ***a scale factor which*** is used to scale ***the gate***'s output load driving capability and its input pin loads. ***The area of the sized gate*** is determined by equation (5). area of sized gate=S*(area of gate) (5) ***The area of the*** mapped digital circuit ***can be estimated*** based on ***the sum*** of the ***total areas of the sized gates plus the net area*** (which is ***estimated from the total length of all nets*** in the circuit).
SYNOPSYS DRAFT PAT. APP. AT 16-17 We can do this by ***calculat***ing single parameter per net, called the ***net weight***, which ***represents the sensitivity of the total area of*** the network ***with respect to the load*** on that ***net***. This ***net weight*** can be calculated in a manner that is very similar to the calculation of the pin loads during the area calculation above. Starting at ***the primary inputs, the net weight of*** the first (left-most) ***gate is equal to its area per unit load. The net weights of the other*** cells can now be ***calculated*** with a recurrence relation traversing the network from left to right.	**'446 PATENT AT 12:22-30** Thus, the following discussion now turns to the ***calculat***ion of "***net weights***." The ***net weight represents the sensitivity of the total area of*** a digital circuit ***with respect to the load*** of a particular ***net***. As an example, ***the net weight*** of a given ***gate***, which is immediately coupled to ***the primary inputs*** of a digital circuit, ***is equal to its area per unit load***. Using equation (6), ***the net weight of the other*** gates in the digital circuit are then ***calculated*** in a leveled order towards the primary outputs of the digital circuit.

Synopsys Draft Patent Application[1]	Specification Of `446 Patent (Also Contained in '438 Patent)
SYNOPSYS DRAFT PAT. APP. AT 17 The ***buffering*** algorithm works as follows: First it finds ***locations in the*** network ***where a buffer can be added*** without increasing the network delay. This is done ***by subtracting the delay of the buffer from the local slack, to give the predicted slack after buffer insertion. If the predicted slack is larger then the network slack, then a buffer*** can be ***inserted without increasing the*** network ***delay.***	**`446 PATENT AT 13:23-37** The ***buffering*** step of 215 (FIG. 4) is discussed in further detail with reference to FIG. 8. In step 650, ***locations in the*** circuit are determined ***where a buffer can be added*** so that buffer insertion will still permit timing constraints to be met. This determination is made ***by subtracting the delay of the buffer from the "local slack", to give the*** value of the ***predicted slack after buffer insertion.*** Slack is zero or positive if the timing constraints are met. In addition, all slacks in the circuit can be summarized by the "network slack" which is the single "worst" slack number. If the network slack is non-negative, then timing closure is achieved. ***If the predicted slack*** calculated in step 650 ***is larger than the network slack, then*** it is possible to ***insert*** a ***buffer without increasing the*** circuit ***delay.***
SYNOPSYS DRAFT PAT. APP. AT 17-18 Next we have to calculate the reduction in load of this net, and check that ***area*** that is ***added*** by adding the ***buffer does not exceed the area saved by sizing down the source gate.*** The ***area added by inserting the buffer is*** simply ***the area of the buffer*** times its ***size, where the size is determined by the load*** on the buffer ***divided by the typical load*** of ***the buffer. The area saved by*** **inserting** the ***buffer*** can be calculated by first ***calculating the change in load due to the insertion*** of the buffer: ***some sinks are removed, the input load of the buffer is added, and the*** net load estimate ***may change*** as a result of the ***number of fanouts of the*** net ***changing.***	**`446 PATENT AT 13:37-48** In step 655, it is determined whether the ***added area*** due to ***buffer*** insertion ***does not exceed the area saved by sizing down the source gate.*** The ***added area*** (***by inserting the buffer) is*** equal to ***the area of the buffer*** multiplied by the buffer ***size, wherein the buffer size is determined by the*** buffer ***load*** C ***divided by the typical load*** C/S on ***the buffer. The area saved by*** sizing down the source gate is determined by first ***calculating the change in net load due to the buffer insertion.*** This ***net load change*** is due to the following: (1) ***some sinks*** (which sink currents***) are removed,*** (2) ***the input load of the buffer is added, and*** (3) ***the number of fanouts of the gate may change.***

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SYNOPSYS DRAFT PAT. APP. AT 18 ***After the buffer*** is ***inserted, the capacitances need to be updated in the fanin cone of the buffer, while the net weights need to be updated in the fanout cone of the buffer.***	**`446 PATENT AT 13:53-57** ***After the buffer*** has been ***inserted***, then in step 670 ***the capacitance*** values ***need to be updated in the fanin cone of the buffer, while the net weights need to be updated in the fanout cone of the buffer.***
SYNOPSYS DRAFT PAT. APP. AT 18 The next step is the process of "***Stretch***ing" and "***Compress***ing" ***the delays of the individual gates to meet the*** timing ***constraints. Gates which are on long paths*** which do ***not meet the delay constraint are "compressed" until the path*** does ***meet the*** timing ***constraint. Gates on*** the ***short paths which easily meet the*** timing ***constraints are "Stretched". Gates with stretched delays require less area for the same load.*** In this step the ***delay*** of the ***gates*** is traded against the ***gain*** of the ***gates***. When ***the delay of*** a ***gate*** decreases so does the gain of the gate. It is important that there is enough gain in the network.	**`446 PATENT AT 14:20-36** Prior to cell placement, ***the delays of the individual gates*** may be ***stretch***ed or ***compress***ed ***to meet the*** delay ***constraints***, as shown in step 220 of FIG. 4. As shown in FIG. 9A, by compressing (decreasing) the delay of a given gate, the gate gain decreases. ***Gates which are on long paths not meet***ing ***the delay constraint***s ***are compressed*** (in delay) ***until the*** long ***path***s ***meet the*** delay ***constraint***s. The ***delay*** of the ***gate***s (or gate) may be decreased as long as the minimum required gain requirements are met. By stretching (increasing) the delay of a given gate, the ***gate gain*** increases (see FIG. 9A). ***Gates on short paths which easily meet the*** delay ***constraints are stretched*** (in delay), since ***gates with stretched delays require less area for the same load. The delay of*** the gates (or ***gate***) in a path are stretched to the extent that timing constraints for the digital circuit are still met.
SYNOPSYS DRAFT PAT. APP. AT 18-19 ***For the purpose of stretching and compressing registers*** can usually be ***considered*** to be ***part of a path which they originate, but not of*** a ***path*** that ***they terminate.***	**`446 PATENT AT 15:48-51** ***For the purpose of stretching and compressing, registers*** in the circuit are preferably ***considered*** as ***part of a path*** from ***which they originate, but not part of*** the ***path*** from which ***they terminate.***
SYNOPSYS DRAFT PAT. APP. AT 19 The stretching algorithm considers the cells ***on a path by path basis***, processing the ***path*** with the smallest slack ***first.***	**`446 PATENT AT 15:9-10** The invention operates ***on a path-by-path basis*** whereby the most critical ***path*** in a digital circuit 750 is evaluated ***first.***

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SYNOPSYS DRAFT PAT. APP. AT 19 After a cell ***has been adjusted***, ***it becomes "locked"*** and its ***delay*** can***not be*** changed by the ***stretching*** algorithm.	**`446 PATENT AT 15:21-25** After the gate 754 ***has been adjusted*** to meet the Path 2 timing constraints, ***it becomes "locked,"*** whereby the gate 754 delay will ***not be*** adjusted further for the remainder of the compression and ***stretching*** step.

EXHIBIT E

UNITED STATES DISTRICT COURT

NORTHERN DISTRICT OF CALIFORNIA

SAN FRANCISCO DIVISION

SYNOPSYS, INC., a Delaware corporation,

Plaintiff,

vs.

MAGMA DESIGN AUTOMATION, INC. a Delaware corporation,

Defendant.

CASE NO. C-04-03923 MMC

DECLARATION OF LUKAS VAN GINNEKEN

I, Lukas van Ginneken, have personal knowledge of the statements and facts set forth herein and do hereby declare under penalty of perjury under the laws of the State of California and the United States of America that the following is true and correct:

1. In 1995, I was hired by Synopsys, Inc. ("Synopsys") to work in the development of Synopsys' logic synthesis and related technologies. I was given the responsibility to work on research pertaining to logic synthesis, and was asked to make contributions to the technical vision for Synopsys' logic synthesis team. I understood that, given my prior experience in the field, Synopsys was relying upon me to provide leadership and vision to the development of Synopsys' products and technology.

2. On or about May 17, 1995, I signed a Proprietary Information and Inventions

3/10/05

Agreement (the "Agreement"; attached as Exhibit "1" hereto). I understood that signing the Agreement was a condition to my employment by Synopsys.

3. I know of no reason why the Agreement is not valid and fully enforceable against me.

4. As reflected in the attachment marked as Exhibit "A" to the Agreement, I attached a list of "inventions or improvements" which I had contributed to before my employment at Synopsys. I believed then, and continue to believe now, that this list was accurate except for patents and patent applications and research reports in which I was involved at IBM.

5. Neither the patents, patent applications and research reports in which I was involved at IBM nor the inventions or improvements listed in Exhibit "A" to the Agreement disclose the inventions ultimately claimed in U.S. Patent No. 6,453,446 or U.S. Patent No. 6,725,438 (hereinafter collectively referred to as the "Patents"). In fact, I did not conceive of any of the inventions disclosed in the Patents before I joined Synopsys.

6. After signing the Agreement, I started my employment at Synopsys on or about June 26, 1995.

7. At no time during my employment at Synopsys, or anytime thereafter, did I object to the scope or terms of the Agreement, or ask Synopsys for any waiver from the enforcement of its provisions.

8. In early 1996, as part of my job to research and explore new product ideas for Synopsys, I conceived the idea of creating an Electronic Design Automation ("EDA") product that would use the concept of fixed timing.

9. Under the concept of fixed timing, the timing delays of a chip design are held constant and "fixed," in contrast to determining timing delay at a later point in the design flow. Because fixed timing involves holding the timing delay constant, it can also been referred to as "constant delay."

10. The inventions I conceived while employed by Synopsys were designed to implement this concept of fixed timing/constant delay into an EDA tool that performed logic synthesis, placement, and/or related tasks. These were the same inventions that were later disclosed in the Patents.

3/10/05

11. In addition, by early 1996, I had conceived of inventions while employed by Synopsys pertaining to the use of "gain-based synthesis," which is one of the ways in which the fixed timing concept can be implemented in a logic synthesis and/or placement tool.

12. In early 1996, I participated in a meeting with other Synopsys personnel to discuss ideas for Synopsys' next-generation synthesis product (code named "NGSS" or "Synzilla"). During this meeting, I set out the basic concept for my fixed timing inventions. I was directed to research the issue further and report my findings at a later meeting.

13. During a subsequent meeting in 1996, I gave a further presentation to Synopsys personnel concerning the inventions I developed while employed at Synopsys. During the meeting, I discussed how Synopsys could implement the inventions in its tools. During the course of this meeting, I was successful in convincing others at Synopsys that the company should consider redirecting its efforts towards implementing these inventions.

14. It is my understanding that the conception of the inventions I developed while a Synopsys employee is thoroughly documented in Synopsys' records.

15. In early 1996, I filled out an invention disclosure form (attached as Exhibit "2" hereto) attesting that my fixed timing inventions were conceived by myself alone. This invention disclosure, under the title "Constant Delay Synthesis" (the "Constant Delay Synthesis Disclosure"), states as follows:

> Constant delay synthesis is an entirely different paradigm for delay optimization in logic synthesis. It promises to radically simplify the design process from behavioral synthesis down to physical desing [sic]. It is probably more of a philosophy than an algorithm. Using this philosophy many common optimization algorithms, such as mapping, retiming, behavioral synthesis, delay [&] area optimization, placement can be reformulated in a much simpler form.

16. In the Constant Delay Synthesis Disclosure, I truthfully represented my understanding that I was the sole inventor of the fixed timing inventions as described in the disclosure form..

17. In the Constant Delay Synthesis Disclosure, I truthfully represent that the fixed timing inventions were being considered as the "cornerstone" of the NGSS project at Synopsys.

18. In the Constant Delay Synthesis Disclosure, I stated my understanding that "[i]t is

important that Synopsys acquires patent protection in this area, even though some prior art exists."

19. It is my understanding that my conception of these inventions while employed at Synopsys is further documented in the performance reviews I received at Synopsys. For instance, in my performance review for the period March 1, 1996 to April 1, 1997 (attached as Exhibit "3" hereto), Synopsys stated that "[o]ver the past year within the Advanced Technology Group, you have had basically one objective: driving through the next generation synthesis effort based on constant delay." The review further stated:

> "Your primary objective over the past year has been driving the technical direction of the Synzilla project, bringing to fruition your ideas on applying constant delay to Synopsys next generation synthesis effort. This project represents a major milestone and direction for Synopsys, and your efforts have been instrumental in effecting the project. One year ago, Synzilla was an idea in your head; it is currently a staffed project that has met aggressive milestones and schedules and that has strong support from outside partners."

20. Similarly, another of my performance reviews (attached as Exhibit "4" hereto) accurately discussed the presentation of the fixed timing inventions in one of the internal Synopsys meetings in early 1996:

> "Lukas, you demonstrated true vision and original thinking in one of the NGSS meetings when you presented your 'constant delay' ideas. I think that in the process of one hour, you presented a change in the synthesis paradigm to the best technical minds at Synopsys, they accepted that the idea has a lot of merit, and the team initiated a project to investigate this further. This is really exciting!"

21. In order to obtain patent protection for the fixed timing and gain-based synthesis inventions I conceived while employed at Synopsys, I proceeded to work with Synopsys' patent counsel in order to draft a patent application. A patent application was ultimately drafted containing the same inventions that were later disclosed in the Patents.

22. One draft of the patent application (attached as Exhibit "5" hereto) was entitled "System and Method for Constant Delay Synthesis," and contained disclosure of my inventions for fixed timing, including use of fixed timing in relation to logic synthesis and placement, equal slack sizing, area estimation, buffering, bipartitioning, iterative placement, and net weights. All of the inventions contained in this application were solely conceived by me at Synopsys. I never disclosed this draft patent application to the public, and I have no reason to believe that it was not maintained by Synopsys as proprietary and confidential.

3/10/05

23. After the creation of this draft, work on the application continued, and eventually a subsequent draft was created. This draft (attached as Exhibit "6" hereto) was entitled "Method for Achieving Timing Closure of Digital Networks and Method for Area Optimization of Digital Networks Under Timing Closure." This draft more thoroughly disclosed the inventions I conceived of while employed at Synopsys, and described in detail the use of fixed timing in relation to network slack, library independent optimization, mapping for delay, post mapping optimization, pin swapping, boundary moves, area estimation, net weights, buffering, stretching, placement, partitioning, and final or discrete sizing. All of the inventions contained in this application were solely conceived by me at Synopsys. I never disclosed this draft patent application to the public, and I have no reason to believe that it was not maintained by Synopsys as proprietary and confidential.

24. In addition to the preparation of the draft patent applications, I also authored a "white paper" on the fixed timing inventions. The white paper was titled "The Constant Delay Methodology," and set forth several aspects of the inventions contained in the Patents. This paper contained, for instance, a description of the use of fixed timing as it related to logical effort and gain, sizing and placement, buffering, transition time effects, area optimization, and area estimation. The end of the paper recommended that Synopsys adopt the fixed timing methodology for its tools.

25. After this white paper was created, I authored a new paper with the title "Driving on the Left-Hand Side of the Performance Speedway." Once again, this paper provided a description of numerous aspects of the inventions I conceived of that are contained in the Patents.

26. I understand that, as the above indicates, by the middle of 1996 Synopsys had extensive confidential documentation describing, in great detail, inventions I conceived while employed at Synopsys. Synopsys did not ever give me permission to take or use this documentation, or any of the inventions described therein, for the benefit of another company. To the contrary, I understood that under the Agreement the inventions that I conceived were and are the property of Synopsys, and were assigned to Synopsys the instant that they were conceived.

27. At some point in 1997, I decided to resign from Synopsys to pursue other opportunities. Instead, however, of pursuing ideas at another company that were unrelated to Synopsys' confidential information, I was offered another position where I could continue utilizing

the inventions I conceived at Synopsys.

28. In May of 1997, I formally resigned from Synopsys in order to join Magma, which had been incorporated on April 1, 1997. In my resignation letter, I stated that I was resigning to join a "newly formed startup company," and stated that my departure "should not be construed as a lack of faith in the technical approaches which I have been advocating."

29. I have reason to believe that, at a minimum, my supervisor at Magma knew that the fixed timing inventions Magma was intending to use were conceived by myself at Synopsys, and were encompassed by my Agreement with Synopsys.

30. I used for Magma's benefit the inventions contained in Synopsys' draft patent applications, and the inventions from these applications ultimately formed the basis for the patent applications I helped prepare for Magma. I also used for Magma's benefit my knowledge of the information contained in at least one of the white papers that I had created for Synopsys.

31. Magma and I used the inventions that I conceived while employed at Synopsys as a technical foundation for Magma's products.

32. At no time did Synopsys ever provide me, or, to my knowledge, Magma, any permission to take Synopsys inventions or related information.

33. Beginning in 1997, Magma proceeded to extensively use the inventions and information described in the Synopsys draft patent applications and confidential white paper in order to create the patent applications that would ultimately result in the issuance of the Patents.

34. During the course of using the inventions belonging to Synopsys, Magma labeled these inventions as Magma's "FixedTiming" methodology. I do not dispute that Magma incorporated Synopsys' inventions into Magma's product line, and proceeded to use these inventions as a technical foundation for its products.

35. As of July 1997, Magma was in possession of inventions and information set forth in the confidential patent applications drafted for Synopsys.

36. In a letter from Pillsbury dated August 18, 1997 (Exhibit "7" hereto), through Magma's legal counsel, Magma and I made the following representations and assurances to Synopsys: (1) "Dr. van Ginneken intends to honor his obligations under his Proprietary Information

Agreement with Synopsys," (2) "Magma is in the practice of taking appropriate steps to protect . . . the trade secrets of its employees' former employers," (3) "Dr. van Ginneken will protect Synopsys' proprietary information during his employment at Magma," (4) "Magma is confident that Dr. van Ginneken has and will continue to abide by the terms of the Magma Agreement in the performance of his duties for Magma," and (5) "Magma will reiterate to Dr. van Ginneken his duty to abide by his Synopsys Agreement." At the time that this letter was sent, I knew that at least statements (1) and (3) above were false. In addition, at or about the time these statements were made, Magma already was using the inventions and information from the confidential patent applications drafted for Synopsys (and information contained in at least one confidential Synopsys white paper).

37. In 1998, I was interviewed by an individual named Marios Papaefthymiou, who I understood had been tasked with determining the extent to which Magma employees had used information from my prior employers. Neither Magma, to my knowledge, nor I informed Mr. Papaefthymiou of the fact that Magma's patent applications contained Synopsys' inventions and confidential information.

38. From 1997 to the present, Magma has prosecuted patent applications disclosing inventions owned by Synopsys and using the same language that also is contained in Synopsys confidential documents. These applications include the applications that ultimately issued as the '446 Patent and '438 Patent.

39. In a declaration signed by me on or about May 4, 1998, and submitted to the Patent and Trademark Office by Magma, I represented under oath that I was the "original, first and sole inventor" of the inventions claimed in the '446 Patent.

40. In a declaration signed by me on or about July 1, 1997, I represented under oath to the United States Patent and Trademark Office that Narendra Shenoy and I were the original, first, and sole inventors of the inventions disclosed in the '114 Patent.

41. Though I conceived the Inventions while employed at Synopsys, the Inventions were not implemented by Synopsys or the Synopsys-IBM joint development team before I resigned from Synopsys.

42. The Inventions were conceived by myself during my employment for Synopsys for

3/10/05

the purpose of developing Synopsys' products.

43. I understand that on or about April 23, 2002, Patent No. 6,378,114, entitled "Method for the Physical Placement of an Integrated Circuit Adaptive to Netlist Changes," was issued to Synopsys. I am a named inventor on the '114 Patent.

44. I understand that on or about September 17, 2002, the '446 Patent, entitled "Timing Closure Methodology," was issued to Magma. The '446 Patent discloses inventions which I conceived while employed at Synopsys.

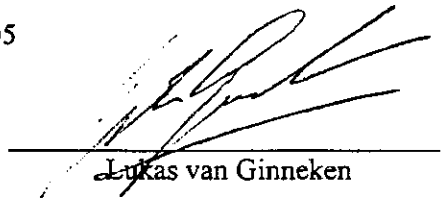
45. I understand that on or about April 20, 2004, the '438 Patent, entitled "Timing Closure Methodology," was issued to Magma. The '438 Patent discloses inventions which I conceived while employed at Synopsys.

46. I breached my obligations to Synopsys under the Agreement by, among other things, (a) failing to keep proprietary information of Synopsys in trust and confidence, and (b) using and disclosing Synopsys' proprietary information to and on behalf of Magma without the written consent of Synopsys.

47. Without waiving any attorney client privilege, I confirm that I am signing this Declaration of my own free will, after having consulted with my counsel regarding the nature, purpose and effect of this Declaration.

I DECLARE UNDER PENALTY OF PERJURY UNDER THE LAWS OF THE STATE OF CALIFORNIA AND THE UNITED STATES OF AMERICA THAT ALL OF THE FOREGOING STATEMENTS AND FACTS CONTAINED HEREIN ARE TRUE AND CORRECT.

Dated: March 10, 2005



3/10/05

Lukas van Ginneken

EXHIBIT F

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March 7, 2006

VIA HAND DELIVERY

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Re: *Synopsys v. Magma, et al.*
Case No.: USDC D. Del. No.: 05 00701 GMS

Dear Mr. Pooley:

This letter respectfully requests that Magma immediately dismiss with prejudice its claim for infringement of the '328 Patent. Our investigation has revealed the existence of a wealth of prior art that clearly invalidates the '328 Patent, none of which was disclosed by Magma to the PTO. Though we are prepared to serve and file an appropriate Rule 11 motion, we are confident that Magma will realize it must voluntarily dismiss its infringement claim without the necessity of such a motion.

We have located dozens of different pieces of prior art that we believe invalidate the '328 Patent. This letter will focus on three examples: the OCTTools program, the CHDStd system, and the IBM integrated data model. As discussed below, it is frivolous for Magma to maintain its infringement claim in the face of this prior art.

1. **The OCTTools Program**. Since at least the early 1990's, a tool has been available on the Internet which performs all of the elements of the claims of the '328 Patent. This tool integrates synthesis, placement, and other EDA programs into a common data model, and permits area-based queries using KD trees. Attached hereto as Exhibit A is a copy of the user guide and reference guide for Version 5.2 of the OCTTools program (note the cover date of 5/25/93). Also attached as Exhibit B is documentation concerning the "region package" for the program, demonstrating the program's use of area-based queries. Also attached as Exhibit C is documentation concerning the KD geometrical data structure package used by the OCTTools program. Note that this documentation makes reference to prior papers by authors Rosenberg and Bentley, which describe performance of region queries using KD tree data structures. Attached as Exhibit D is a copy of papers by Rosenberg and Bentley on this subject. We also direct your attention to the website http://embedded.eecs.berkeley.edu/pubs/

downloads/octtools, which contains the published source code for the program (with copyright dates in the mid-1990s). We cannot fathom how Magma could seriously contend that the inventions in the '328 Patent are valid in light of this prior art.

2. **CHDStd System**. Several years before the '328 Patent was filed, SEMATECH member companies developed the Chip Hierarchical Design System (CHDS), which involved a common data model shared between different EDA tools and programs. Our investigation has confirmed that the CHDS contains the elements of the claims of the '328 Patent, including an area-based query using a hierarchical tree structure. Attached as Exhibit E is a copy of a paper on CHDS standards, published in 1998 by authors associated with the Silicon Integration Initiative ("Si2") and IBM Corporation. Also attached as Exhibit F is an EETimes article, published in 1996, which further discusses CHDS. We would also direct your attention to Si2's website, which includes an archive of materials available at http://archives.si2.org/si2_publications/CHDStd/PDF/. The Si2 organization has posted CHDS materials on its website since 1996. We cannot understand how Magma could possibly maintain its infringement claim in good faith in the face of this prior art. We also cannot understand how Magma could justify its failure to disclose this common data model (which was well-known to Magma and other companies throughout the EDA industry) during the several years the patent was pending before the PTO.

3. **The IBM Integrated Data Model**. Many years before the '328 Patent was filed, IBM generated its Integrated Data Model ("IDM") which involved a common data model shared between different EDA tools and programs. This unified data model had been developed by IBM at the time of Dr. van Ginneken's employment there, and in fact Dr. van Ginneken was directed to work on this model during his employment at IBM. Attached as Exhibit G is a paper, published in the IBM Journal of Research and Development in 1996, discussing IBM's Integrated Data Model. Note also that SEMATECH selected IDM as the basis for development of the CHDS standards. *See* Exhibit E. In addition, Dr. van Ginneken also had access to IDM information as a result of his work at Synopsys. Incredibly, the existence of the IDM was not disclosed to the PTO during prosecution of the '328 Patent, despite van Ginneken's prior knowledge of this data model while at both IBM and Synopsys. Since the elements of the claims of the '328 Patent were practiced by IDM, this data model also entirely invalidates the '328 Patent.

4. **Other Materials**. Magma cannot deny that the idea of performing an area query based on a KD tree has been used in EDA applications since the 1980's. For instance, attached as Exhibit H is a paper by Lai et al., that compares the use of linked lists, quad trees and KD trees for performing area queries in VLSI CAD tools. It is

Dechert LLP

unfortunate that during prosecution of the '328 Patent, Magma never disclosed this or other similar references to the PTO.

Please note that the above does not take into account the prior art that exists with respect to Synopsys/Avant!'s own products. As you know, we believe that Magma's claims are frivolous because the very products that it claims infringes the '328 Patent were performing in the same way well before the '328 Patent was even filed. However, there is no need to raise this issue for purposes of this letter, since the above prior art fully suffices to invalidate all the patent claims.

In light of the above (and numerous other instances of prior art located in our investigation which we will be providing to you), Magma's '328 Patent is clearly invalid. After reviewing this prior art, Magma must realize that it has a Rule 11 obligation to dismiss its infringement claim. We expect Magma to do so immediately.

Lastly, I understand that, during your conversation with Chris Graham today, you were informed of the existence of this prior art but nevertheless inquired whether Synopsys would continue to gather further documents relating to Magma's infringement claim. It clearly makes no sense, however, to continue placing burdens on Synopsys with respect to this claim, when the evidence of the invalidity of the '328 Patent is so clear. Magma cannot use the assertion of a clearly invalid patent as a basis to conduct a fishing expedition through Synopsys's files.

In light of the huge burden imposed by Magma's pending requests, we need an immediate confirmation from Magma that it will dismiss its infringement claim. Given the discovery burdens Magma would otherwise seek to impose on Synopsys, we request that you confirm Magma's withdrawal of its infringement claim no later than March 15, 2006. If Magma provides this confirmation as we believe it must pursuant to Rule 11, this would render Magma's request for source code and other materials moot. If Magma does not provide this confirmation, but instead insists on utilizing the '328 Patent as an basis to place burdens on Synopsys, we intend to seek reimbursement of all fees and costs spent in litigating Magma's infringement claim.

Very truly yours,

Michael N. Edelman

MNE/cas

EXHIBIT G

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April 24, 2006

VIA HAND DELIVERY

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Re: *Synopsys v. Magma, et al.*
Case No.: USDC D. Del. No.: 05 00701 GMS

Dear Mr. Pooley:

This follows up on the letter of March 7, 2006 from Michael Edelman, in which we requested that Magma dismiss with prejudice its claim for infringement of the '328 Patent in light of prior art that was attached to the letter, including the OCTTools Program, the Chip Hierarchical Design System ("CHDS") and IBM's Integrated Data Model ("IDM"). After reviewing the prior art attached to Mr. Edelman's previous letter, Magma should have clearly understood that it has a Rule 11 obligation to dismiss its infringement claim. Although Magma has had ample time to review the prior art, it has yet to dismiss its infringement claim, and it has yet to provide any good faith explanation as to why Magma's '328 Patent is not clearly invalid in light of this prior art.

As explained in Mr. Edelman's March 7 letter, the OCTTools Program integrates synthesis, placement, and other EDA programs into a common data model, and permits area-based queries using KD trees. *See* Exhibit A to March 7 letter. Our continued investigation has revealed the existence of even more evidence that the OCTTools Program clearly invalidates the '328 Patent. For instance, please find attached the following additional prior art references:

- Rick Spickelmier and Brian Richards, "The OCT Data Manager," Anatomy of a Silicon Compiler, Robert W. Brodersen, editor. Kluwer Academic Publishers, Boston, 1992 (the "OCT Data Manager Text Book"), attached hereto as Exhibit A;
- Timothy Barnes, David Harrison, A. Richard Newton, and Rick L. Spickelmier, "Electronic CAD Frameworks," Kluwer Academic Publishers, Boston, 1992 (the "CAD Frameworks Text Book"), attached hereto as Exhibit B;

- Rick L. Spickelmier, "The Application of Knowledge-Based Systems to Design Verification," UCB/ERL M89/126, Electronics Research Laboratory, University of California, Berkeley, California, November 1989. Ph.D Thesis (the "Spickelmier Ph.D. Thesis"), attached hereto as Exhibit C.

- David S. Harrison, Peter Moore, Rick L. Spickelmier and A. Richard Newton, "Data Management and Graphics Editing in the Berkeley Design Environment," The Proceedings of IEEE ICCAD, Santa Clara, CA, pp. 20-24, November 1986 (the "BERKELEY DESIGN ENVIRONMENT PAPER"), a copy of which is attached hereto as Exhibit D.

The OCT Data Manager Text Book and the Spickelmier Ph.D. Thesis provide further description of the Oct Data Manager, which is the common data model underlying the OCTTools. These references leave no doubt that that the Oct Data Manager practiced all the limitations of the claims in the `328 patent.

The only basis that Magma has articulated pertaining to validity of the '328 Patent is a vague contention in response to Synopsys' interrogatory. *See* Defendant Magma Design Automation, Inc.'s Response To Plaintiff Synopsys' Second Set of Interrogatories [Nos. 6-14], served on April 6, 2006. Synopsys' interrogatory asked for ***all*** facts and evidence supporting the contention that Magma is not practiced or disclosed by prior art. In its response, all that Magma could come up with was the following:

> This ***invention claimed in the '328 patent is a model for representing a circuit that is capable of being utilized throughout the different stages of the design process, from behavioral synthesis to placement and routing***. The object in the model, once associated with a physical location, are also subsequently adapted for retrieval using an area query. ***At least one of the following elements, among others, are missing from the prior art: adaptation for retrieval using an area query and the ability to use the same model from behavioral synthesis to placement and routing***.

Id. at pp. 15-16.

Magma cannot seriously contend, however, that the feature of "adaptation for retrieval using an area query" is not found in the OCT data manager. The use of area queries to retrieve objects in a common data model is explicitly discussed in the OCT documentation. *See* Exhibit B to March 7 letter (documentation for OCTTools "region package"). Further, the adaptation of objects for area queries was also well-known by anyone with ordinary skill in the art, as the wealth of prior art indicates. *See, e.g.*, "Multidimensional Binary Search Trees used for Associative Searching," Jon Louis

Bentley, CACM, Vol. 18, No. 9, pp. 509-517, Sept. 1975; and "Geographical Data Structures Compared: A Study Of Data Structures Supporting Region Queries," Jonathan Rosenberg, IEEE Transactions on Computer-Aided Design, Vol. CAD-4, No. 1, January 1985, copies of which are attached to the March 7 letter.

Magma's interrogatory cites "the ability to use the same model from behavioral synthesis to placement and routing." First, we have no idea how Magma derives this limitation, as it does not appear anywhere in the patent claims. In any event, even assuming this could somehow constitute a claim limitation, this ability was also a well-documented feature of the OCT data manager. The OCT Data Manager Text Book provides a precise description of this feature:

> OCT, an object oriented database designed for VLSI applications, which had been under development for some time was then incorporated as the underlying database. This immediately gave access to a number of new tools which were already interfaced to OCT. In addition, the X windows interface was adopted and ***policies were adopted for the use of the OCT database so that data could be stored from high level flow graphs through to the actual physical design***.

Exhibit A, OCT Data Manager Text Book, p. 4 (emphasis added). The OCT Data Manager Text Book further explains:

> The generation tools in LAGER can be divided into two basic categories which perform ***behavioral synthesis*** and silicon assembly. The ***behavioral synthesis*** components are exemplified by `Hyper`, `Firgen` and `C-to-Silicon`. These take a behavioral input, which is relatively hardware independent, that describes the specification desired by the designer. They output a structural description (interconnection of circuit blocks and their parameters), which provides the input to the silicon assembly tools. These tools implement the actual ***physical design*** which can be used for fabrication, and include `Flint.Tim-Lager`, `dpp`, `Padroute`, and `Stdcell` and are controlled by `DMoct`.

Exhibit A, OCT Data Manager Text Book, p. 5. Indeed, all one need do is run the OCTTools program (which has been publicly available on the Internet for years), to see that it does indeed "use the same model from behavioral synthesis to placement and routing."

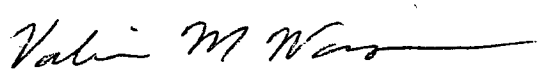
Indeed, the prior art Synopsys has provided is only the beginning; precisely the same "distinguishing" features that Magma identified in its interrogatory response are

also contained in a series of other prior art we have identified. In addition, to the extent they may be contained in any Synopsys product, they were being performed by Synopsys long before the patent was filed. In light of the multitude of prior art, Magma's continued prosecution of an infringement claim predicated on an obviously invalid patent is inexcusable.

Unless and until Magma withdraws its '328 Patent infringement claim, Synopsys will have no choice but to incur significant costs, and expend significant resources, in defending itself against a patent that Magma itself now knows is invalid. Outside of filing a Rule 11 motion, which Synopsys intends to do, there is nothing more that Synopsys can do now to force Magma to comply with its ethical obligations and dismiss the infringement claim. But we intend to keep sending you these letters, as we want the record to be absolutely clear that every dollar Synopsys has to spend in defense of Magma's frivolous claim is a dollar wasted.

Magma should bear in mind not only Synopsys' plans to seek reimbursement for the costs it has needlessly incurred defending against this invalid patent, but also the malicious prosecution implications that are clearly involved. We will continue to remind you of Magma's Rule 11 obligations until and unless this patent claim is dismissed with prejudice.

Very truly yours,



Valerie M. Wagner

VMW/cas

Enclosures